RESPONSE UNDER 37 C.F.R. § 1.116
EXPEDITED PROCEDURE
GROUP ART UNIT 2173

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No: 09/832,997 §
Filed: April 10, 2001 §
Inventor(s): §
Adam Gabbert and Jeff Washington §
§
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§
§
Title: SYSTEM AND METHOD §
FOR CREATING A §
GRAPHICAL PROGRAM §
INCLUDING A PLURALITY §
OF PORTIONS TO BE §
EXECUTED
SEQUENTIALLY

Examiner: Bonshock, Dennis
Group/Art Unit: 2173
Atty. Dkt. No: 5150-49000

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, Alexandria, VA 22313-1450, on the date indicated below.

Jeffrey C. Hood

Signature — August 5, 2005 Date

REQUEST FOR PRE-APPEAL BRIEF REVIEW

ATTN: BOX AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request. This request is being filed with a Notice of Appeal. The review is requested for the reason(s) stated below.

Applicant is in receipt of the Office Action mailed May 5, 2005. Claims 1-31 remain pending in the present case. Reconsideration of the present case is earnestly requested in light of the following remarks. Please note that for brevity, only the primary arguments directed to the independent claims are presented, and that additional arguments, e.g., directed to the subject matter of the dependent claims, will be presented if and when the case proceeds to Appeal.

Claims 1-10 and 13-31 were rejected under 35 U.S.C. 102(b) as being anticipated by Kaiser et al. (U.S. Patent No. 4,970,664, hereinafter "Kaiser"). Claims 11 and 12 were rejected under 35 U.S.C. as

being unpatentable over Kaiser and Kodosky et al. (U.S. Pat. No. 5,301,301, hereinafter "Kodosky"). Applicant respectfully traverses these rejections.

The present claims relate to the field of graphical software programming. As described in detail in the Description of the Related Art in the present application, a user may create a graphical program by including a plurality of nodes or icons in a block diagram and interconnecting the nodes to accomplish a desired function or process. The plurality of interconnected nodes visually indicate functionality of the graphical program, e.g., the function or process performed by the graphical program. The graphical program may be executed on a computer system to perform the function or process.

More particularly, the present claims relate to a method enabling a user to specify a sequential order of execution for different portions of the graphical program. For example, claim 1 recites as follows:

> 1. (Previously Presented) A method for creating a graphical program including a plurality of portions of graphical source code to be executed sequentially, the method comprising:
>
> displaying a plurality of frames in the graphical program such that two or more frames are visible at the same time, wherein the graphical program comprises a plurality of interconnected graphical program nodes that graphically represents functionality of the graphical program, and wherein the graphical program is executable by a computer system to perform the functionality;
>
> including a portion of graphical source code in each frame in response to user input;
>
> wherein for each frame, said including a portion of graphical source code in the frame in response to user input comprises including one or more graphical program nodes in the frame in response to user input;
>
> wherein the plurality of frames define an execution order for the plurality of portions of graphical source code such that during execution of the graphical program the plurality of portions of graphical source code are executed sequentially in accordance with the execution order defined by the plurality of frames.

Thus, a plurality of frames are displayed in the graphical program such that two or more frames are visible at the same time. The user includes a portion of graphical source code (i.e., one or more nodes) in each of the frames. The plurality of frames define an execution order for the portions of graphical source code. Thus, when the graphical program is executed, the frames cause the portions of graphical source code to be executed sequentially in accordance with this execution order defined by the frames.

Applicant submits that Kaiser cannot possibly teach the combination of elements recited in claim 1 because Kaiser does not even teach the concept of a graphical program. Kaiser relates generally to a critical path analyzer for an electronic circuit. A designer utilizes a schematic editor to create a design of a hardware circuit. For example, the designer may interact with the schematic editor to create a graphical representation of the circuit by selecting various component symbols from a library and creating

connections between the component symbols. (See Col. 3, line 31 – Col. 4, line 2). A critical path analyzer accepts the circuit data from the schematic editor, defines signal paths from that data, and determines which of the signal paths are critical in terms of timing (Col. 4, lines 5-9).

Applicant notes that a graphical representation of a hardware circuit as taught in Kaiser is not a graphical program as recited in claim 1. Claim 1 recites that, "the graphical program is executable by a computer system to perform the functionality", i.e., the functionality that is graphically represented by the interconnected graphical program nodes. However, a graphical representation of a circuit as taught in Kaiser is not executable by a computer system. A graphical representation of a circuit is a model of a hardware design. The circuit representation is not a software program, and Kaiser nowhere describes it as being a software program. In contrast, the graphical program recited in claim 1 is a software program executable by a computer system.

The Examiner states that, "With regard to claim 1, further teaching the graphical program having a plurality of interconnected nodes, Kaiser teaches, in column 3, line 34 through column 4, line 2, a plurality of sheets connected to each other sheets comprising components connected by wire connections." However, this section of Kaiser describes the process of the designer interacting with the schematic editor to create a graphical representation of a circuit, as described above. The "components" refer to hardware components of the circuit. As described above, the graphical representation of the hardware circuit is not the same as a graphical software program, and in particular, the components in the graphical representation do not represent program code that is executable by a computer system.

The Examiner asserts that, "With regard to claim 1, further teaching the program being executable on a computer system, Kaiser teaches, in column 3, lines 30 through column 4, line 2, a graphical program made up of instructions, executable by the computer system." However, Applicant respectfully disagrees. Kaiser simply does not teach that the circuit design created by the schematic editor is made up of instructions executable by a computer system. The cited portion of Kaiser does not refer to anything that is "made up of instructions" or "executable by the computer system", as asserted by the Examiner. Kaiser instead teaches at Col. 3, line 66 – Col. 4, line 9 that the schematic editor produces circuit data (not instructions) that can then be accessed (not executed) by other design automation packages such as fault simulators, logic simulators, and timing analyzers.

Claim 1 further recites the limitation of, "including a portion of graphical source code in each frame in response to user input; wherein for each frame, said including a portion of graphical source code in the frame in response to user input comprises including one or more graphical program nodes in the frame in response to user input". With regard to this claim limitation, the Examiner states that, "Kaiser teaches, in column 3, line 60 through column 4, line 2, the circuit data, comprising different components connected by wires, being entered graphically by the designer." Applicant agrees that this portion of

Kaiser teaches circuit data, comprising different components connected by wires, being entered graphically by the designer. However, Kaiser does not teach the designer including a portion of circuit data in each of a plurality of frames in the circuit design. The cited portion of Kaiser contains no teaching whatsoever regarding a plurality of frames.

The Examiner states that, "With regard to claim 1, further teaching displaying a plurality of frames in the graphical program such that two or more frames are visible at the same time, Kaiser teaches, in column 2, lines 20-24 and in figure 2, two or more frames visible together." Figure 2 of Kaiser illustrates a path context window that has a number of display portions of variable width for displaying path portions from separate schematic sheets. Applicant notes that the display portions appear on the screen display after the designer has created the circuit design using the schematic editor and run a critical path analysis with a critical path analyzer. (See Col. 4, lines 16-61). Therefore, if the display portions shown in Figure 2 are taken to mean the "frames" recited in claim 1 then Kaiser clearly cannot teach the limitation of, "including a portion of graphical source code in each frame in response to user input". In order to include a portion of circuit data in each display portion, the display portions would need to be visible at the time the designer is creating the circuit design. However, Kaiser clearly teaches that the display portions appear after the designer has created the circuit design. Furthermore, Kaiser contains no teaching whatsoever regarding the designer including different portions of circuit data in different display portions or frames.

Claim 1 further recites the limitation of, "wherein the plurality of frames define an execution order for the plurality of portions of graphical source code". The Examiner states that these features are taught at Col. 2, lines 20-24 and Col. 1, lines 30-42. However, Col. 1, lines 30-42 is simply background information pertaining to critical delays in a circuit. Col. 2, lines 20-24 simply states that Kaiser's apparatus "displays in a screen display a signal path entirely, the signal path having portions that appear on separate schematic sheets". Neither of the cited sections teach a plurality of frames that define an execution order for a plurality of portions of graphical source code. Furthermore, Applicant submits that Kaiser's display portions do not define an execution order for different portions of the signal path. As described at Col. 4, line 16 – Col. 5, line 50, each of Kaiser's display portions simply displays a portion of a signal path that is located on a separate schematic sheet. Thus, by displaying the display portions adjacent to each other, the user can view an entire signal path, whereas prior analyzers only showed one path portion at a time. However, the execution of the signal path is defined entirely by the circuit design itself, which is created before the display portions are ever displayed on the screen display. The execution of the signal path is not influenced by the display portions at all. In particular, the display portions do not define an order of execution for the various path portions displayed in the display portions.

Thus, for at least the reasons provided above, Applicant submits that Kaiser does not teach numerous elements of claim 1, and thus, claim 1 and those claims dependent thereon are allowable over the cited art. Inasmuch as claims 14 and 21 recite similar elements as claim 1, Applicant submits that these claims and the claims dependent thereon are also allowable. Furthermore, many of the dependent claims include further limitations not taught or suggested by Kaiserand/or Kodosky. However, since the independent claims have been shown to be patentably distinct, a further discussion of the dependent claims is not necessary at this time.

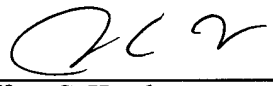
In light of the foregoing amendments and remarks, Applicant submits the application is now in condition for allowance, and an early notice to that effect is requested. If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert & Goetzel PC Deposit Account No. 50-1505/5150-49000/JCH.

Also enclosed herewith are the following items:

☒ Return Receipt Postcard

☒ Notice of Appeal

Respectfully submitted,



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Date: 8/5/2005 JCH/JLB